What is claimed is:

1. A semiconductor device comprising:

a semiconductor substrate of a first conductivity type;

a semiconductor layer of a first conductivity type formed on a first main surface of the semiconductor substrate, the semiconductor layer including a first region for a cell portion and a second region for a terminating portion, the second region being positioned in an outer periphery of the first region, said terminating portion maintaining breakdown voltage by extending a depletion layer to relieve an electric field;

junction pairs of semiconductor layers periodically arranged so as to form a line from the first region to the second region in a first direction parallel to the first main surface in the semiconductor layer and having mutually opposite conductivity types of impurities, each of said junction pair being composed of a first impurity diffusion layer of a second conductivity type formed from a surface of the semiconductor layer toward the semiconductor substrate and a second impurity diffusion layer of a first conductivity type formed from the surface of the semiconductor layer toward the semiconductor substrate and adjacently to the first impurity diffusion layer;

a base layer of a second conductivity type selectively formed on each surface layer of said junction pairs which are formed in the first region, so as to connect with the first impurity diffusion layer and the second impurity diffusion layer in the same manner;

a source layer of a first conductivity type selectively formed on each surface layer of the base layers of the second conductive type;

a control electrode formed above each surface of the base layers and above each surface of the source layers via an insulating film;

a first main electrode formed so as to cover the control electrode and to contact the source layers and the base layers in the same manner; and

a second main electrode formed on a second main surface

opposite to the first main surface of the semiconductor substrate.

2. The semiconductor device according to claim 1, which further comprises:

a first dielectric formed from the surface of the semiconductor layer toward the semiconductor substrate in the first region so as to fill a first trench, each of the first trenches having a stripe plane shape and a longitudinal direction of each of the first trenches being a second direction orthogonal to the first direction; and

a second dielectric formed from the surface of the semiconductor layer toward the semiconductor substrate in the second region so as to fill second trenches periodically arranged at least in the second direction,

wherein the junction pair in the first region is formed between the adjacent second dielectrics, and

the junction pairs in the second region include at least a junction pair composed of a cell peripheral impurity diffusion layer which is the impurity diffusion layer formed from an outer side face of the first trench closest to a peripheral edge in the first direction toward the peripheral edge and an impurity diffusion layer formed from the side face closest to the first region among side faces of the second trench toward the first region and having an conductivity type opposite to that of the cell peripheral impurity diffusion layer.

3. The semiconductor device according to claim 2,

wherein the second trenches have a plane stripe shape, longitudinal directions of the second trenches being the same as the first direction.

4. The semiconductor device according to claim 2,

wherein the second trenches have a rectangular plane shape, respectively, and are periodically arranged in the first and second directions so as to form a lattice in a plane view, and

said junction pairs are arranged up to side faces on the

first region side of the second trenches positioned closest to the peripheral edge.

5. The semiconductor device according to claim 3,

wherein the first trenches are formed to extend in the second direction from the first region to the vicinity of a peripheral edge of the second region, and

said junction pairs in the first region are extended in the second direction up to the peripheral edge of the second region, and the extended portions constitute the junction pairs in the terminating portion in the second direction.

6. The semiconductor device according to claim 4,

wherein the first trenches are formed to extend in the second direction from the first region to the vicinity of a peripheral edge of the second region, and

said junction pairs in the first region are extended in the second direction up to the peripheral edge of the second region, and the extended portions constitute the junction pairs in the terminating portion in the second direction.

7. The semiconductor device according to claim 2, which further comprises:

a third impurity diffusion layer of a first conductivity type formed from the surface of the semiconductor layer toward the semiconductor substrate in a peripheral edge portion in the first direction.

8. The semiconductor device according to claim 2, which further comprises:

a fourth impurity diffusion layer of a second conductivity type formed from the surface of the semiconductor layer toward the semiconductor substrate in the peripheral edge portion in the first direction.

9. The semiconductor device according to claim 1,

wherein the junction pairs are formed so as to contact the semiconductor substrate.

10. The semiconductor device according to claim 1, which further comprises:

a field insulating layer provided on a surface of the terminating portion.